REMARKS

By the present amendment, independent claims 1, 9, and 21 have been amended. Reconsideration and allowance of outstanding claims 1-9 and 11-28 in view of the above amendments and following remarks are requested. Applicants respectfully point out to the Examiner that claim 10 was canceled in response to the Office Action dated November 5, 2003.

A. Rejection of Claims 1-3, 7-9, 21-23, and 27-28 under 35 USC §102(e)

The Examiner has rejected claims 1-3, 7-9, 21-23, and 27-28 under 35 USC §102(b) as being anticipated by U.S. Patent Number 5,574,939 to Keckler, et al. ("Keckler"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 9, and 21, is patentably distinguishable over Keckler.

Various embodiments according to the present invention relate to an improved performance VLIW processor. Some previous attempts at VLIW processors result in an advantage in parallel processing of a large number of instructions. Nevertheless, these VLIW processors exhibit unnecessary power consumption while permitting the execution of only a single issue group per clock cycle.

Furthermore, conventional VLIW processors require a relatively large chip area and extra power for an instruction bus that wider than necessary. In a typical

conventional VLIW processor, it takes four clock cycles to execute two VLIW packets each of which include two issue groups, for example.

In contrast to the conventional approaches, in embodiments according to the present invention, two VLIW packets are executed in only two clock cycles with little or no increase in consumed power. A reason for this achievement is that the present system achieves simultaneous execution of, for example, two independent issue groups belonging to different VLIW packets.

As disclosed in the present application, referring to pages 19 and 20 and Figure 3, one embodiment of the present invention teaches the utilization of two processing units, i.e., thread A processing unit 303 and thread B processing unit 305, in contrast to a single processing unit used in the conventional VLIW processors. The unique architecture and issue grouping of the present system results in a doubling of the execution speed of the VLIW processor, in one embodiment. Nevertheless, this doubling of the execution speed does not result in a doubling of the consumed power or increased chip area, as described in the present application at, for example, pages 23 and 24. Consequently, the present system differs from prior attempts to increase the processing speed of VLIW processors.

Amended independent claim 1 recites language indicating that, in one embodiment, each of a first plurality of threads comprises one of a second plurality of processing units. Each of a fourth plurality of instruction packets comprises a third plurality of issue groups. Each of the threads receives a respective issue group and executes the issue groups in a single clock cycle. Amended independent claims 9 and 21

recite similar limitations. Inherent in the amended independent claims is the idea of simultaneous execution of, for example, two independent issue groups belonging to different VLIW packets.

For example, amended independent claim 1 recites that "at least two issue groups of said third plurality of issue groups are from different instruction packets of said fourth plurality of instruction packets." Amended independent claim 9 recites that "said first instruction packet is a different instruction packet than said second instruction packet". Amended independent claim 21 recites that "at least two issue groups of said second plurality of issue groups are from different instruction packets of said first plurality of instruction packets".

In contrast to the present invention as defined by amended independent claims 1, 9, and 21, Keckler discloses a plurality of processing units, wherein each processing unit comprises a synchronizer for selecting one of a plurality of threads of computation for execution in that unit. Although operations can be executed in parallel, Keckler does not teach simultaneous execution of two or more independent issue groups belonging to different VLIW packets. Therefore, Keckler does not disclose, teach, or suggest the present invention as defined by amended independent claims 1, 9, and 21.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claims 1, 9, and 23 is not taught, disclosed, or suggested by the art of record. Thus, amended independent claims 1, 9, and 23 are patentably distinguishable over the art of record. As such, the claims depending from

amended independent claims 1, 9, and 23 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejections of Claims 4-6, 11-20, and 24-26 under 35 USC §103(a)

The Examiner has rejected claims 4-6, 11-20, and 24-26 under 35 USC §103(a) as being obvious with respect to Keckler in view of alleged "Applicants' admitted prior art." Applicants respectfully submit that claims 4-6, 11-20, and 24-26 depend from amended independent claims 1, 9, and 21, and thus, claims 4-6, 11-20, and 24-26 should be allowed at least for the same reasons discussed above in conjunction with patentability of amended independent claims 1, 9, and 21.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 9, and 21, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-9 and 11-28 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-9 and 11-28 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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